DRAFT

1026

Proposal for Memory-to-Memory Transfer Unit

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MEMORANDUM FOR FILE

I. Introduction

The MMTU consists of two DR11-B DMA units connected "back to back" through an interface unit. The two UNIBUS parts of the MMTU may be connected to the same UNIBUS, for Memory-to-Memory transfers within a machine, or to two different UNIBUSes for transfers between machines.

The MMTU is completely symmetrical, that is, its structure is identical on each end. For convenience in the following discussion we will label the ends "A" and "B". To transfer data from "A" to "B" we must set up a "transmit" command in "A" and a "receive" command in "B".

II. Bus Interface

The following discussion describes the bus interface of the "A" end. The "B" end is identical.

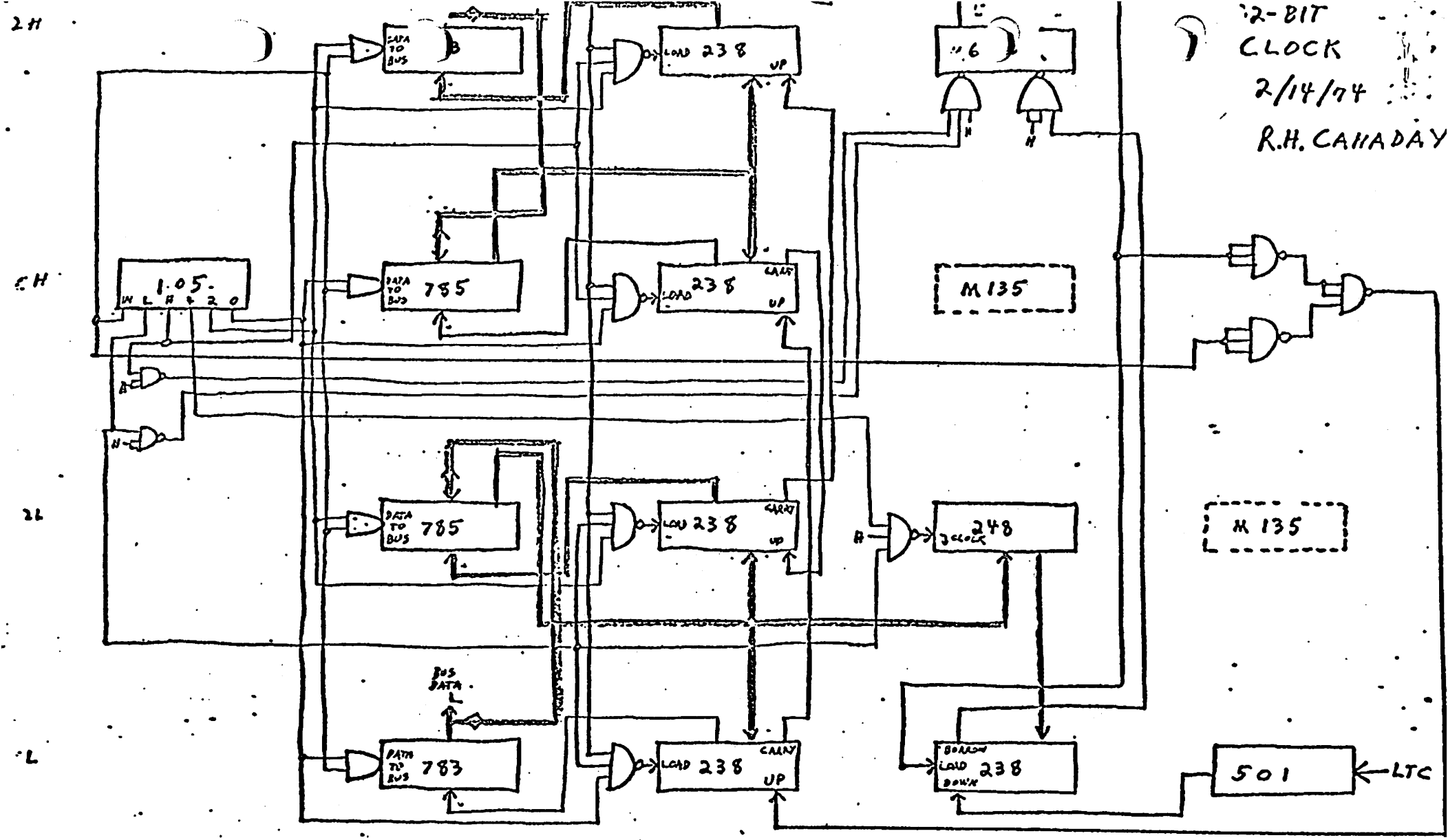
There are 4 addressable 16-bit registers in "A". These are:

Bus Address: Bit 00 is ignored and replaced by 0. Thus transfers are always on a word boundary. Bits 01-15, plus two bits from the Status and Control register (q.v.) make up the extended bus address for the transfer, normally a memory address.

The attached diagram shows interconnections between the DEC M-series modules (see DIGITAL Logic Handbook 1973-74, from DEC, for specifications of each module). The orange lines represent 8-bit-wide data paths. UNIBUS connections to the M105 address selector module are not shown (see Logic Handbook).

RR-9152-RHC-ds Rudd H. Canaday

Att.


12-BIT
CLOCK
2/14/74
R.H. CAHADAY
2H
6H
2L
L
105
DATA TO BUS
785
783
LOAD 238
CARRY
UP
M135
248
BORROW
LOAD DOWN
501
LTC
BUS DATA L